WHAT IS CLAIMED IS:

1. An integrated circuit comprising a first impedance termination circuit, the first impedance termination circuit comprising:

a first termination resistor coupled to a first input/output pin on the integrated circuit;

a common mode driver; and

a first transistor coupled between the first termination resistor and the common mode driver, the first transistor blocking current flow through the first termination resistor when the first transistor is OFF,

wherein a body of the first transistor is coupled to a first supply voltage.

2. The integrated circuit according to claim 1 further comprising:

a second transistor coupled in parallel with the first transistor that blocks current flow through the first termination resistor when the first and the second transistors are OFF,

wherein a body of the second transistor is coupled to a second supply voltage.

3. The integrated circuit according to claim 1 wherein the first impedance termination circuit further comprises:

a first pass gate coupled in parallel with the first termination resistor.

4. The integrated circuit according to claim 3 wherein the first termination impedance circuit further comprises:

a second pass gate coupled in parallel with the first termination resistor and the first pass gate.

5. The integrated circuit according to claim 3 wherein a second termination resistor is coupled in series with the first termination resistor and the first pass gate.

6. The integrated circuit according to claim 1 further comprising a second impedance termination circuit, the second impedance termination circuit comprising:

a second termination resistor coupled to a second input/output pin on the integrated circuit; and

second and third transistors coupled in parallel between the second termination resistor and the common mode driver, the second and the third transistors blocking current flow through the second termination resistor when the second and the third transistors are OFF,

wherein a body of the second transistor is coupled to the first supply voltage, and a body of the third transistor is coupled to a second supply voltage.

7. The integrated circuit according to claim 6 wherein the second impedance termination circuit further comprises:

first and second pass gates coupled in parallel with the second termination resistor; and

a third termination resistor coupled in series between the second termination resistor and the second pin.

8. The integrated circuit according to claim 6 further comprising a third impedance termination circuit, the third impedance termination circuit comprising:

a third termination resistor coupled to the first input/output pin; and

fourth and fifth transistors coupled in parallel between the third termination resistor and the common mode driver, the fourth and the fifth transistors blocking current flow through the third termination resistor when the fourth and the fifth transistors are OFF,

wherein a body of the fourth transistor is coupled to the first supply voltage, and a body of the fifth transistor is coupled to the second supply voltage.

9. The integrated circuit according to claim 8 further comprising a fourth impedance termination circuit, the fourth impedance termination circuit comprising:

a fourth termination resistor coupled to the second input/output pin; and

sixth and seventh transistors coupled in parallel between the fourth termination resistor and the common mode driver, the sixth and the seventh transistors blocking current flow through the fourth termination resistor when the sixth and the seventh transistors are OFF,

wherein a body of the sixth transistor is coupled to the first supply voltage, and a body of the seventh transistor is coupled to the second supply voltage.

10. The integrated circuit according to claim 1 wherein the integrated circuit is a field programmable gate array.

11. A method for providing termination impedance to a first pin using a first termination resistor on an integrated circuit, the method comprising:

turning OFF a first pass gate to block current through the first termination resistor on the integrated circuit, wherein the first pass gate includes first and second transistors;

driving a voltage on the first pin to high and low supply voltages while the first pass gate is OFF; and

preventing leakage current from flowing through drain/source-to-body diodes of the first and the second transistors while the first pass gate is OFF.

12. The method as defined in claim 11 wherein preventing the leakage current from flowing further comprises:

coupling a body region of the first transistor to the high supply voltage and a body region of the second transistor to the low supply voltage.

13. The method as defined in claim 11 further comprising:

turning ON the first pass gate to provide a current path through the termination resistors; and

turning ON a second pass gate coupled in parallel with the first termination resistor.

14. The method as defined in claim 13 further comprising:

turning ON a third pass gate coupled in parallel with the first termination resistor, wherein a second termination resistor is coupled between the first pin and the first termination resistor.

15. The method as defined in claim 11 further comprising:

turning OFF a second pass gate to block current through a second termination resistor on the integrated circuit, wherein the second termination resistor provides termination impedance to a second pin, and the first pass gate includes third and fourth transistors;

driving a voltage on the second pin to the high and the low supply voltages while the second pass gate is OFF; and

preventing leakage current from flowing through drain/source-to-body diodes of the third and the fourth transistors while the second pass gate is OFF.

16. The method as defined in claim 15 wherein the first and the second pass gates are coupled to a common mode driver.

17. The method as defined in claim 15 wherein preventing the leakage current from flowing through the third and the fourth transistors further comprises:

coupling a body region of the third transistor to the high supply voltage and a body region of the fourth transistor to the low supply voltage.

18. A method for providing termination impedance on an integrated circuit, the method comprising:

providing a current path through a first on-chip resistor to a pin of the integrated circuit;

blocking current flow through the first on-chip resistor by turning OFF a first transistor; and

preventing source/drain-to-body diodes of the first transistor from becoming forward biased in response to voltage changes on the pin.

19. The method of claim 18 wherein preventing the source/drain-to-body diodes of the first transistor from becoming forward biased further comprises:

coupling a body region of the first transistor to a first supply voltage.

20. The method of claim 19 wherein blocking the current flow through the first on-chip resistor further comprises:

turning OFF a second transistor coupled in parallel with the first transistor; and

preventing the source/drain-to-body diodes of the second transistor from becoming forward biased in response to voltage changes on the pin.

21. The method of claim 20 wherein preventing the source/drain-to-body diodes of the second transistor from becoming forward biased further comprises:

coupling a body region of the second transistor to a second supply voltage.